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METHOD FOR MANUFACTURING A MULTI-BIT MEMORY CELL

Cross-Reference to Related Application:

This is a divisional of U.S. application No. 10/352,826, filed January 28, 2003, now Patent No. 6,673,677, which was a continuation of International Application PCT/DE01/02811, filed July 25, 2001, which designated the United States, and which was not published in English.

Background of the Invention:

Field of the Invention:

The present invention relates to a manufacturing method for a multi-bit memory cell with self-adjusting ONO regions.

In U.S. Patent No. 5,768,192, a non-volatile memory is described in which electrons are trapped at a source region or a drain region respectively in a memory layer. The trapped electrons determine a threshold voltage of the transistor, which is configured as a semiconductor oxide nitride oxide semiconductor (SONOS) transistor. The presence of a charge at the source or drain respectively can be interpreted as a stored bit so that two bits can be stored in a cell of this kind. For programming, hot charge carriers are produced in the channel; the electrons are injected near to the drain